In the Claims:

1-18. (cancelled)

19. (new) A process of selecting alternative test circuitry within an integrated circuit comprising:

A. shifting instruction data into an instruction register of a test access port, the instruction data including information for selecting the alternative test circuitry;

B. outputting from the instruction register instruction data for selecting the alternative test circuitry;

C. performing an instruction update operation at the end of the shifting;

D. selecting the alternative test circuitry in response to the outputting and performing.

20. (new) The process of claim 19 including stepping a finite-state test access port controller through states to perform the instruction update operation.

21. (new) The process of claim 19 including stepping a finite-state test access port controller through states to perform the shifting.

22. (new) The process of claim 19 in which the outputting includes outputting from the instruction register an instruction data signal for selecting the alternative test circuitry, and the performing includes outputting an instruction update signal from a test access port controller.

23. (new) The process of claim 19 in which the outputting includes outputting from the instruction register an instruction data signal for selecting the alternative test circuitry, the performing includes outputting an instruction update signal from a test access port controller, and the

selecting includes selecting the alternative test circuitry in response to the instruction data signal and the instruction update signal.